**WHAT IS CLAIMED IS:**

1. A multiplier circuit comprising:

a partial products generating circuit capable of receiving a multiplicand value and a multiplier value and generating therefrom a plurality of partial products;

a first summation array circuit comprising a first plurality of adders capable of summing a first subset of said plurality of partial products to thereby produce a first summation value; and

a second summation array circuit comprising a second plurality of adders capable of summing a remaining subset of said plurality of partial products to thereby produce a second summation value, wherein said remaining subset of said plurality of partial products comprises all of said plurality of partial products not included in said first subset of said plurality of partial products.

2. The multiplier circuit as set forth in Claim 1 wherein said first subset comprises even ones of said plurality of partial products.

3. The multiplier circuit as set forth in Claim 2 wherein said remaining subset comprises odd ones of said plurality of partial products.

4. The multiplier circuit as set forth in Claim 3 wherein each of said first and second pluralities of adders comprises a carry-save adder.

5. The multiplier circuit as set forth in Claim 4 further comprising a final stage carry-save adder capable of summing said first summation value and said second summation value.

6. The multiplier circuit as set forth in Claim 5 wherein said first summation value comprises a first N-bit sum value and a first N-bit carry value and said second summation value comprises a second N-bit sum value and a second N-bit carry value and wherein said final stage carry-save adder compresses said first and second summation values to produce a final summation value comprising a final N-bit sum value and a final N-bit carry value.

7. The multiplier circuit as set forth in Claim 6 further comprising a carry-propagate adder capable of adding said final N-bit sum value and said final N-bit carry value to produce a 64-bit resulting sum value and a 1-bit resulting carry value.

8. The multiplier circuit as set forth in Claim 7 wherein said multiplier circuit is disposed in at least one of a floating point unit and an integer unit in a data processor.

9. A data processor comprising a plurality of pipelined execution units, said pipelined execution units comprising at least one of a floating point unit and an integer having at least one multiplier circuit therein, wherein said at least one multiplier circuit comprises:

a partial products generating circuit capable of receiving a multiplicand value and a multiplier value and generating therefrom a plurality of partial products;

a first summation array circuit comprising a first plurality of adders capable of summing a first subset of said plurality of partial products to thereby produce a first summation value; and

a second summation array circuit comprising a second plurality of adders capable of summing a remaining subset of said plurality of partial products to thereby produce a second summation value, wherein said remaining subset of said plurality of partial products comprises all of said plurality of partial products not included in said first subset of said plurality of partial products.

10. The data processor as set forth in Claim 9 wherein said first subset comprises even ones of said plurality of partial products.

11. The data processor as set forth in Claim 10 wherein said remaining subset comprises odd ones of said plurality of partial products.

12. The data processor as set forth in Claim 11 wherein each of said first and second pluralities of adders comprises a carry-save adder.

13. The data processor as set forth in Claim 12 further comprising a final stage carry-save adder capable of summing said first summation value and said second summation value.

14. The data processor as set forth in Claim 13 wherein said first summation value comprises a first N-bit sum value and a first N-bit carry value and said second summation value comprises a second N-bit sum value and a second N-bit carry value and wherein said final stage carry-save adder compresses said first and second summation values to produce a final summation value comprising a final N-bit sum value and a final N-bit carry value.

15. The data processor as set forth in Claim 14 further comprising a carry-propagate adder capable of adding said final N-bit sum value and said final N-bit carry value to produce a 64-bit resulting sum value and a 1-bit resulting carry value.

16. The data processor as set forth in Claim 15 wherein said at least one multiplier circuit comprises a first multiplier disposed in said floating point unit and a second multiplier disposed in said integer unit.

17. For use in a data processor, a method of multiplying a multiplicand value and a multiplier value comprising the steps of:

generating a plurality of partial products from the multiplicand value and the multiplier value;

summing a first subset of the plurality of partial products in a first summation array circuit to thereby produce a first summation value; and

summing a remaining subset of the plurality of partial products in a second plurality of adders to thereby produce a second summation value, wherein the remaining subset of the plurality of partial products comprises all of the plurality of partial products not included in the first subset of the plurality of partial products.

18. The method as set forth in Claim 17 wherein the first subset comprises even ones of the plurality of partial products.

19. The method as set forth in Claim 18 wherein the remaining subset comprises odd ones of the plurality of partial products.

20. The method as set forth in Claim 19 wherein each of the first and second pluralities of adders comprises a carry-save adder.